REMARKS

Claims 1-5, 13-14, 19-22 and 25 will be pending upon entry of the present amendment. Claims 1-2 and 13-25 are rejected. Claims 3-5 are objected to. Claims 1-5, 13 and 19 are being amended. Claim 15-18 and 23-24 are being cancelled. No new matter is presented.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

Claim Objections

On page 2 of the Office Action, the Examiner objected to claim 2 because of an informality. In response, Applicants are amending claim 2 by replacing the phrase "output voltage signal from said plurality of VRMs; said second supply voltage reference" with the phrase "output voltage signal from said plurality of VRMs and said second supply voltage reference." Applicants respectfully request that the objection be withdrawn.

Claim Rejections under 35 U.S.C. § 112

On page 2, the Examiner rejected claim 2 under 35 U.S.C. § 112, first paragraph. Specifically, the Examiner rejected claim 2 for reciting a controller that supplies an "internal control voltage." In response, Applicant has amended claim 2 by eliminating reference to the "controller," and amended claim 1 by limiting a controller with the phrase "for supplying an **internal control current** to said equivalent droop resistor" (emphasis added).

On page 4, the Examiner rejected claims 1 and 2 under 35 U.S.C. § 112, second paragraph. Referring to claim 1, the Examiner stated that the phrases "receiving an output current signal (Iout) from said plurality of VRMs" and "being connected to said common bus" render the claim as being indefinite. In response, Applicants have deleted the cited phrases from the body of the claim. Referring to claim 2, the Examiner stated that the phrase "arranged to output a control voltage signal to said plurality of VRMs" render claim 2 as being indefinite. In response, Applicants have eliminated the cited phrase from the body of the claim.

Applicants respectfully submit that claims 1 and 2, as amended, remedy any deficiencies under 35 U.S.C. § 112, first and second paragraphs, and request the rejections be withdrawn.

Claim Rejections under 35 U.S.C. § 102

On page 3, the Examiner rejected claim 1 under 35 U.S.C. § 102(b) as being anticipated by *Chesavage* (U.S. Patent No. 5,834,925). Applicants respectfully traverse.

Applicants have amended claim 1 by adding some elements recited in claim 2, and limiting the "controller" as recited in claim 2. Amended claim 1 recites, in part,

> first and second control resistors connected, in series with each other, to said common bus to receive said output current signal; a third summing node, being input a first local control voltage from said first control resistor as a positive addend and a second local control voltage from said second control resistor as a negative addend; and a controller connected to an output of said third summing node and said equivalent droop resistor for supplying an internal control current to said equivalent droop resistor.

Applicants submit that *Chesavage* does **not** disclose either all the elements as claimed or the connections between the elements as claimed. For example, *Chesavage* does not disclose "first and second control resistors connected, in series with each other, to said common bus to receive said output current signal," as claimed. *Chesavage* does illustrate (Fig. 4) a common output connected to the total current sensor 59 (Fig. 4) that receives current from each power supply 60a, 60b and 60c. However, *Chesavage* does **not** disclose resistors connected in series with each other to the common bus to receive the output current signal. It is clear that none of the pairs of resistors (57a and 52a, or 57a and 56a as illustrated in Fig. 4) are first and second control resistors connected in series with each other to a common bus to receive an output current signal, as claimed.

Furthermore, *Chesavage* does **not** disclose a "third summing node, being input a first local control voltage from said first control resistor ... and a second local control voltage from said second control resistor," as claimed. For example, even if resistors 57a and 53a are considered to be first and second resistors connected in series with each other to a common bus to receive an output current signal, Applicants contend that these resistors are not first and

second control resistors since *Chesavage* does not suggest, teach, or disclose a summing node that is input a first local control voltage from resistor 57a and a second local control voltage from resistor 53a.

Finally, *Chesavage* does not disclose a "controller connected to an output of said third summing node and said equivalent droop resistor," as claimed. For example, if the current sensing amplifier 55a as defined by the Examiner is the "controller" and if the local current sensing resistor 56a as defined by the Examiner is the "droop resistor," then as illustrated in Fig. 4 either the resistor 53a, the PWR output stage, or the total current amplifier 59 must act as the "third summing node," since as claimed, "a controller [is] connected to an output of said third summing node and said equivalent droop resistor." However, *Chesavage* does not disclose that either the resistor 53a, the PWR output stage, or the total current amplifier 59 are a "summing node." In fact, it is clear that neither the resistor 53a, the PWR output stage, or the total current amplifier 59 are a "summing node", since none of these elements are input "a first local control voltage from said first control resistor ... and a second local control voltage from said second control resistor," as claimed.

Based at least upon the above remarks, Applicants respectively submit that *Chesavage* does not anticipate amended claim 1, and request that claim 1 be allowed. Furthermore, since claim 2 depends directly from claim 1, Applicants submit that claim 2 as amended is allowable for at least the same reasons given above in conjunction with claim 1, and request that claim 2 be allowed.

On page 4, the Examiner rejected claims 13-25 under 35 U.S.C. § 102(b) as being anticipated by *Small* (U.S. Patent No. 4,717,833). Applicants respectfully traverse.

Applicants are amending claim 13 by adding the limitations recited in claims 16-18, and amending claim 19 by adding the limitations recited in claims 23-24. In addition, Applicants are further amending claims 13 and 19 by adding the limitation "the first resistor, share resistor, and second resistor being connected in series with each other."

Amended claims 13 and 19 recite, in part,

> ... a share resistor coupled between the common bus and the second input of the second error amplifier; a first resistor connected between the share resistor and the first input of the second error amplifier; and a second resistor connected between the share resistor and the second input of the second error amplifier, the first resistor, share resistor, and second resistor being connected in series with each other.

With regard to claims 17 and 18, the Examiner stated on page 6 of the Office Action that *Small* discloses a "share resistor coupled between the common bus and the second input of the second error amplifier (fig. 1, resistor R2)," a "first resistor connected between the share resistor and the first input of the second error amplifier (fig. 1, resistor R2; fig. 3, resistance of element 36 between R3 and input 3 of parallel amplifier)," and a "second resistor connected between the share resistor and the second input of the second error amplifier (fig. 3, resistor R7 between R3 and input 2)."

With regard to the Examiner's reference to Fig. 1 (*Small*), the Examiner has contended that resistor R2 is both the share resistor and the first resistor, as claimed. However, the Examiner is mistaken, since R2 cannot be both a share resistor and a first resistor, since as claimed, "a first resistor [is] connected between the share resistor and the first input of the second error amplifier ...." In addition, Fig. 1 does not disclose, nor has the Examiner shown, "the first resistor, share resistor, and second resistor being connected in series with each other," where the first resistor is connected to the first input of the second error amplifier and the second resistor is connected to the second input of the second error amplifier, as claimed.

With regard to the Examiner's reference to Fig. 3 (*Small*), the Examiner has contended that the first resistor is the internal resistance of transistor 36, the second resistor is R7, and the share resistor is R3. However, these resistors are not "connected in series with each other," where the first resistor is connected to the first input of the second error amplifier and the second resistor is connected to the second input of the second error amplifier, as claimed.

On page 7 of the Office Action, the Examiner rejected claims 23-24 based upon similar arguments as given in conjunction with the rejections of claims 17-18. Based at least upon the above arguments, Applicants respectfully submit that claims 17-18 and 23-24 are not anticipated by *Small*. Since Applicants have amended claim 13 to recite the limitations of claims 16-18 and

amended claim 19 to recite the limitations of claims 23-24, Applicants respectfully submit that claims 13 and 19 are not anticipated by *Small*.

Furthermore, with regard to claim 13, the Examiner stated that *Small* discloses a first current generator (i.e., resistor R8) coupled to the first input of the first error amplifier 22 (Fig. 1). However, Applicants submit that resistor R8 is **not** a current generator, but is a feedback resistor that couples the output of amplifier 22 to one of the inputs of amplifier 22. The feedback resistor R8 is an essential component that allows amplifier 22 to amplify small voltage differences between the two inputs (+ and -) to amplifier 22 in order to control the output voltage Vout (i.e., to approximate Vout to the reference voltage Vref). For example, *Small* states, col. 4, lines 5-11, "any change of the output voltage from current monitor 12 reflecting a change in load current from the power supply to which the parallel control circuit of FIG. 1 is connected will result in the output signal from amplifier 22 ... changing to maintain V_{out} from power supply equal to V_{ref}." In other words, resistor R8 does not function as a current generator, but functions as a feedback resistor that allows amplifier 22 to amplify a difference signal input to maintain the output voltage V_{out} equal to the reference voltage V_{ref}.

Based at least upon the above remarks, Applicants submit that amended claims 13 and 19 are not anticipated by *Small*, and request that claims 13 and 19 be allowed. In addition, since claims 14 and 25 depend from claim 13, Applicants submit that claims 14 and 25 are allowable based at least upon the reasons given above in conjunction with claim 13, and request that claims 14 and 25 be allowed. Furthermore, since claims 20-22 depend either directly or indirectly from claim 19, Applicants submit that claims 20-22 are allowable based at least upon the reasons given above in conjunction with claim 19, and request that claims 20-22 be allowed.

Allowable Subject Matter

Applicants thank the Examiner for indicating that claims 3-5 would be allowable if rewritten in independent form including the limitations of the base claim and all intervening claims. Applicants respectfully submit that since claims 3-5 depend indirectly from claim 1, claims 3-5 are allowable for at least the same reasons given above in conjunction with claim 1, and request that claims 3-5 be allowed.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

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